IN THE SPECIFICATION:

Please amend the title of the invention on page 1, lines 1 through 2 as follows:

"SYSTEM AND METHOD FOR PARTIAL MERGERS FOR SUB-REGISTER DATA OPERATIONS IN A PROCESSOR"

Please amend the second full paragraph on page 7, lines 10 through 17 as follows:

--To prevent a carryover from the most significant bit of the low-order results of the adder 520 into the least significant bit of the high-order results of the adder 510, an AND gate 580, for example, may be positioned between adders 510 and 520, as shown in FIG. 5. Setting the carry enable 555 to "False" will force a "0" to be output from output 557 of the AND gate 580, thus, preventing the carryover. Accordingly, the higher-order bits of the result are effectively copied from the high-order bits of register 550 (i.e., EAX), while the lower-order bits 551, 561 of each register are added and the results are moved into the low-order locations of register 570, thus, completing the ADD function.--